

AT32F415 OTG New Features

Introduction

This document introduces how to use AT32F415C OTG new features as below:

Feature 1: In OTGFS Device mode, VBUS (PA9) can be configured for use by other peripherals; Set bit[21]=1 in the OTG_FS_GCCFG register to enable feature 1.

Feature 2: In OTG_FS Device mode, endpoint 3 supports remap. Once enabled, it can be used as endpoint 3 and endpoint 4 (depending on the configuration of USB device) to communicate with host simultaneously.

Set $((\text{uint32_t} *)0x40021044) |= 0x80000000$ to enable feature 2.

This sample code applies to Revision C products of AT32F415 series, which integrates ARM™ 32-bit Cortex®-M4 core.

Table 2 lists all product models, and Table 1 lists the identification method of products mentioned in this document.

- Revision code on the device marking
- The last number of product identification on the packaging label

Table 1. MCU identification

Part number	Revision code on device marking
AT32F415	“C”

1. The Flash size information and Bit[78:76] Mask_Version in the unique device ID (UID base address: 0x1FFF F7E8) indicate the revision of MCU. That is, read the Bit[6:4] at address 0x1FFF7F1 to obtain the product revision as below:
Revision B: 0b001
Revision C: 0b010
2. Refer to [Section 2 Silicon version on device marking](#) to identify the revision of product.

Applicable products:

Part number	AT32F415C
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List of peripherals:

Main peripheral	OTG
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1 Application method

1.1 Hardware requirements

- 1) AT-START-F415 evaluation board
- 2) USB interface

1.2 Software requirements

- 1) SourceCode
 - 415_OTG_Device_NewFunction

1.3 Example of feature 1 application (PA9 released)

- 1) Open project\at_start_f415\examples\usb_device\vcp_Loopback_funtion1, compile and download to the evaluation board;
- 2) Use AT-START-F415 evaluation board;
- 3) This routine demonstrates how to release VBUS (PA9) pin for use by other peripherals in OTG Device mode of AT32F415C (PA9 is released for USART in this routine);
- 4) Open the USB_VBUS_IGNORE macro definition, as shown below:

```
/**
 * @brief ignore vbus detection, only available in at32f415xx revision C.
 *
 * at32f415xx revision B: (not support)
 *
 * the vbus detection pin (pa9) can not be used for other functionality.
 *
 * vbus pin must kept at VBUS or VDD.
 *
 *
 * at32f415xx revision C: (support)
 *
 * ignore vbus detection, the internal vbus is always valid.
 *
 * the vbus pin (pa9) can be used for other functionality.
 */
#define USB_VBUS_IGNORE
```

- 5) Download this routine to the target evaluation board, and connect OTG interface to PC. After USB is connected to the host, check whether both the USB and USART can send and receive data normally.

1.4 Example of feature 2 application (used as endpoint 3 and endpoint 4 simultaneously)

- 1) Open project\at_start_f415\examples\usb_device\ custom_hid_funtion2 source code, compile and download to the evaluation board;
- 2) Use AT-START-F415 evaluation board;

- 3) This routine demonstrates how to use endpoint 4 on AT32F415C and use project\at_start_f415\examples\usb_device\Artery_UsbHid_Demo_V1.0.1 host for communication test;
- 4) Part of the sample code is shown below:

```
crm_otgfs_ep3_remap_enable(TRUE);//call this function to enable endpoint 3 remap

//IN transmission through endpoint 3

#define USBD_HID_IN_EPT                0x83
#define USBD_HID_OUT_EPT               0x03

__ALIGNED(4) uint8_t g_usbd_configuration[]={

    ...

    USB_DEVICE_EPT_LEN,
    USB_DESCRIPTOR_TYPE_ENDPOINT,
    USBD_HID_IN_EPT+1, // Enumeration declared to host as endpoint 4
    USB_EPT_DESC_INTERRUPT,
    LBYTE(USB_IN_MAXPACKET_SIZE),
    HBYTE(USB_IN_MAXPACKET_SIZE),
    HID_BINTERVAL_TIME,

    USB_DEVICE_EPT_LEN,
    USB_DESCRIPTOR_TYPE_ENDPOINT,
    USBD_HID_OUT_EPT,
    USB_EPT_DESC_INTERRUPT,
    LBYTE(USB_OUT_MAXPACKET_SIZE),
    HBYTE(USB_OUT_MAXPACKET_SIZE),
    HID_BINTERVAL_TIME,

}
```

- 5) The USB capture result is that endpoint 3 used for OUT and endpoint 4 used for IN, as shown below:

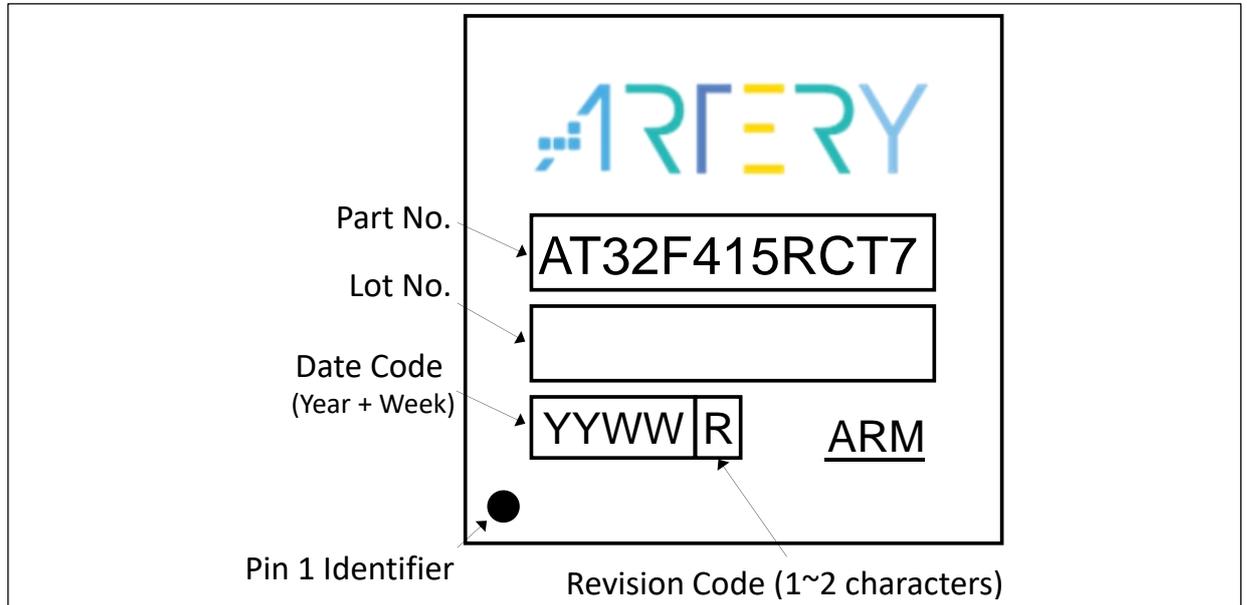
Figure 1. Endpoint communication diagram

Transfer	F	Bulk	ADDR	ENDP	Bytes Transferred	Time	Time Stamp
1	S	OUT	32	3	64	3.998 ms	5 . 659 508 166
Transfer	F	Bulk	ADDR	ENDP	Bytes Transferred	Time	Time Stamp
2	S	IN	32	4	64	562.004 ms	5 . 663 505 850
Transfer	F	Bulk	ADDR	ENDP	Bytes Transferred	Time	Time Stamp
3	S	OUT	32	3	64	3.999 ms	6 . 225 509 566
Transfer	F	Bulk	ADDR	ENDP	Bytes Transferred	Time	Time Stamp
4	S	IN	32	4	64	410.007 ms	6 . 229 508 632
Transfer	F	Bulk	ADDR	ENDP	Bytes Transferred	Time	Time Stamp
5	S	OUT	32	3	64	3.999 ms	6 . 639 515 900
Transfer	F	Bulk	ADDR	ENDP	Bytes Transferred	Time	Time Stamp
6	S	IN	32	4	64	2.040 sec	6 . 643 515 350
Transfer	F	Bulk	ADDR	ENDP	Bytes Transferred	Time	Time Stamp
7	S	OUT	32	3	64	3.998 ms	8 . 683 543 916
Transfer	F	Bulk	ADDR	ENDP	Bytes Transferred	Time	Time Stamp
8	S	IN	32	4	64	162.003 ms	8 . 687 541 816
Transfer	F	Bulk	ADDR	ENDP	Bytes Transferred	Time	Time Stamp
9	S	OUT	32	3	64	3.999 ms	8 . 849 544 950
Transfer	F	Bulk	ADDR	ENDP	Bytes Transferred	Time	Time Stamp
10	S	IN	32	4	64	184.009 ms	8 . 853 543 616

2 Silicon version on device marking

The silicon version of AT32F415 MCUs is shown as below. The “R” represents the revision code and “C” represents Revision C.

Figure 2. Marking example (top view)



3 Revision history

Table 2. Document revision history

Date	Version	Revision note
2021.12.10	2.0.0	Initial release.

